Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL CHOW, ALLEN J. PORTER, DAVID A. STRASSER, ANTONIO ASARO, INDRA LAKSONO, and BILJANA D. SIMSIC

Appeal No. 2001-0513
Application No. 09/096,550

ON BRIEF

Before THOMAS, RUGGIERO, and GROSS, ***Administrative Patent Judges***.

GROSS, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 23, which are all of the claims pending in this application.

Appellants' invention relates to a method and apparatus for decompressing compressed data, including video data that has been compressed in accordance with the MPEG 2 standard. The process involves retrieving components from a non-local memory at a rate that is independent of the rate in which the components were

written into the non-local memory. Claim 8 is illustrative of the claimed invention, and it reads as follows:

8. A compressed data processing module comprises:

memory interface operably coupled to receive components of the compressed data from a non-local memory;

packet processing module operably coupled to the memory interface, wherein the packet processing module retrieves the components from the non-local memory via the memory interface at a rate independent of a rate in which the components were written into the non-local memory;

data processing module operably coupled to the packet processing module, wherein the data processing module receives the retrieved components from the packet processing module and produces therefrom representations of uncompressed data;

pipeline processing module operably coupled to receive motion vector data and the representations of the uncompressed data and to produce therefrom the uncompressed data, wherein the motion vector data is one of the components; and

frame buffer operably coupled to store the uncompressed data.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Artieri	5,579,052	Nov. 26, 1996
Nishiura	5,764,773	Jun. 09, 1998
Mendenhall et al. (Mendenhall)	5,812,760	Sep. 22, 1998 (filed Jun. 25, 1996)
Kim	5,828,425	Oct. 27, 1998 (filed Nov. 25, 1996)

Claims 1, 3, 4, 8, 10, 11, 14 through 16, and 19 through 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Artieri.

Claims 2 and 9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Artieri in view of Nishiura.

Claims 5, 12, 17, and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Artieri in view of Kim.

Claims 6, 7, 13, 18, and 23 stand rejected under 35 U.S.C. § 103 as being unpatentable over Artieri in view of Mendenhall.

Reference is made to the Examiner's Answer (Paper No. 12, mailed August 8, 2000) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 11, filed May 23, 2000) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 1, 3, 4, 8, 10, 11, 14 through 16, and 19 through 21 and the obviousness rejections of claims 2, 5 through 7, 9, 12, 13, 17, 18, 22, and 23.

Each of the independent claims in one form or another recites a retrieval of the components from the non-local memory at a rate independent of a rate in which the components were written into the non-local memory. The examiner asserts (Answer, pages 4-5) that Artieri teaches in column 4, lines 14-20 and column 7, lines 17-21 that "the packet processing module retrieves the components from the non-local memory at a rate independent of a rate in which the components were written into the non-local memory." The cited portions of Artieri are as follows:

> According to an embodiment of the invention, the system includes a variable length decoder (VLD) forming the master processing element; a run-level decoder (RLD) forming a first element of the pipeline circuit and receiving through the parameter bus the packets processed by the VLD . . .

and

> A picture header includes, as mentioned above, a picture type parameter and information on the use of the movement compensation vectors. These parameters are used by the VLD circuit itself to decode the vectors and data of the macro-blocks.

We find nothing in either of the two passages that would suggest retrieving components from the non-local memory at a rate independent of a rate in which the components were written into the non-local memory, as claimed. The examiner further explains

(Answer, pages 10-11) that the VLD and RLD do not read and write data from the local memory at the same rate. However, as pointed out by appellants (Brief, page 15) in Artieri, the write operations of the VLD can be interrupted by the RLD when the latter can no longer receive data to be processed. Therefore, the VLD and RLD of Artieri are dependent upon each other, which means that their respective reading and writing rates must be dependent upon each other.

The examiner (Answer, page 10) also points to column 3, lines 38-43, wherein Artieri states that the system includes "a memory bus controlled by a memory controller to exchange data between the processing elements at rates adapted to the processing rates of these elements." The examiner contends that this passage indicates that the processing rates are independent of each other. However, although Artieri mentions processing rates, nothing in the reproduced passage suggests that the processing rates must be independent of each other. As we find no teaching or suggestion in Artieri of independent rates of writing and reading from non-local memory by elements of the system, Artieri fails to disclose each and every element of the claims. Accordingly, Artieri cannot anticipate the claims, and

we cannot sustain the anticipation rejection of claims 1, 3, 4, 8, 10, 11, 14 through 16, and 19 through 21.

Regarding the obviousness rejections, Nishiura, Kim, and Mendenhall provide no teaching of independent rates of reading and writing to the non-local memory. Therefore, the combinations of Nishiura, Kim, and Mendenhall with Artieri fail to cure the deficiencies of Artieri alone. Therefore, we cannot sustain the obviousness rejections of claims 2, 5 through 7, 9, 12, 13, 17, 18, 22, and 23.

CONCLUSION

The decision of the examiner rejecting claims 1, 3, 4, 8, 10, 11, 14 through 16, and 19 through 21 under 35 U.S.C. § 102(b) and claims 2, 5 through 7, 9, 12, 13, 17, 18, 22, and 23 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)	

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